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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/810,905	03/26/2004	Haowen Bu	TI-36637	9390

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EXAMINER	
STARK, JARRETT J	
ART UNIT	**PAPER NUMBER**
2823	

NOTIFICATION DATE	DELIVERY MODE
04/30/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/810,905	BU ET AL.	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *11-18* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 2/26/2008 directed to the cited prior art references individually have been fully considered but they are not persuasive.

Applicant's arguments with respect to the newly amended claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1–10 and 19 -20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wieczorek et al. (US 2004/0061228 A1) in view of Chen et al. (US 2005/0136583 A1).

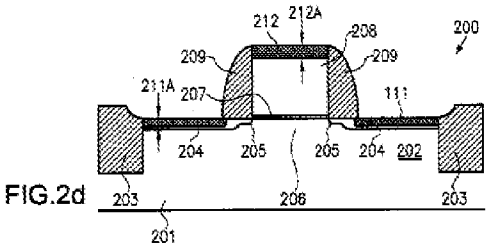

FIG.2d

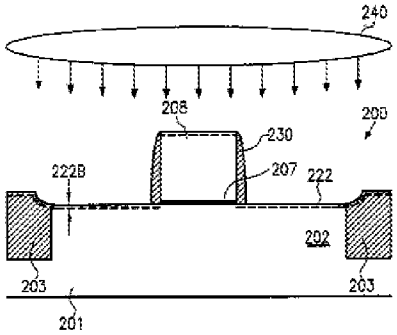

FIG.2e

Regarding claim 1, Wieczorek in view of Chen disclose a method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure (Wieczorek et al., paragraph [0031] -- *Wieczorek et al discloses the invention is intended for forming CMOS transistor elements. CMOS transistor elements are understood in the art to be a pair of symmetrical complimentary transistors one p type and one n type. Wieczorek et al however only shows the general transistor structure, and does not disclose the obvious n/p type doping arrangement that is CMOS technology. It would be obvious to one of ordinary skill in the art that the CMOS structure mentioned by Wieczorek et al. would have a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-*

type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure, because this limitation is the fundamental structure of CMOS.)

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack (Wieczorek et al., Fig. 2d – [205]);

forming a layer of insulating material in contact with a total exposed surface of the lightly-doped extension regions (Wieczorek et al., Fig. 2d – [209]);

forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions (Wieczorek et al., Fig. 2e);

forming at least one sidewall layer coupled to the layer of insulating material;

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks (Wieczorek et al., Fig. 2d – [204]);

Wieczorek et al. does not however disclose the additional step of forming a cap layer. This additional step was however known at the time of the invention to one of ordinary skill in the art. At the time of the invention it was known in that the induced strain/stress in the channel region of a CMOS device can be modified by performing an additional step of cap annealing. This know additional process step when forming a CMOS device is disclosed by Chen et al. Chen discloses the additional steps of:

forming a capping layer of contiguous silicon nitride over the semiconductor substrate (Chen, Fig. 3 - [24]);

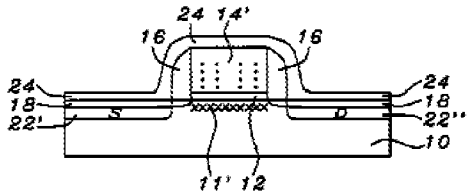

FIG. 3

annealing, after the formation of the capping layer and with the capping layer in place, the extension regions and the source and drain regions (Chen, Fig. 4 - [27] paragraph [0051]); and

removing all of the capping layer after the annealing (Chen, Fig. 5 - [27] paragraph [0059]);

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Wieczorek and Chen to enable the CMOS production step of Wieczorek to be performed according to the teachings of Chen because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed CMOS production step of Wieczorek and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

NOTE: Chen et al. discloses all of the claimed limitations except for the step of implanting a interfacial layer of nitrogen. Additionally, it would be obvious to one of ordinary skill in the art at the time of the invention, in view of Wieczorek, to perform an additional step of forming an interfacial layer of nitrogen within the total exposed surface of the lightly-doped extension regions, merely to achieve the benefits associated to the

silicide formation as disclosed by Wieczorek.

Regarding claims 2-3, Wieczorek in view of Chen disclose the method of claim 1 wherein the extension, source, and drain regions for the PMOS transistors have a dopant concentration in the range of about 1-2 e20 atoms/cm3 (Wieczorek, paragraph [0034]).

Regarding claim 4, Wieczorek in view of Chen disclose the method of claim 1 wherein said interfacial nitride layer has an atomic nitrogen concentration in the range of 2-15 atomic percent (Wieczorek, paragraph [0034]).

Regarding claim 5, Wieczorek in view of Chen disclose the method of claim 1 wherein the insulting layer is selected from the group comprising silicon nitride and silicon oxide (Wieczorek, paragraph [0032-33

Regarding claim 6, Wieczorek in view of Chen disclose the method of claim 1 wherein the step of forming an
interfacial layer of nitrogen is performed using one of the methods selected from the group comprising an NH3 thermal annealing, an NH3 or N2 plasma treatment, or an N implantation (Wieczorek, Fig. 2b).

Regarding claim 7, Wieczorek in view of Chen disclose the method of claim 1 wherein the capping layer has a thickness in the range of 200-1000 angstroms (Chen, paragraph [0048]).

Regarding claim 8, Wieczorek in view of Chen disclose the method of claim 1 wherein the annealing step is performed in the range of 1000-1100 degrees centigrade for a time in the range of less than about 10 seconds (Chen, paragraph [0051] RTA will be below 10 seconds).

Regarding claim 9, Wieczorek in view of Chen disclose the method of claim 1 wherein the step of forming at least one sidewall layer includes the use of a BTBAS precursor (Chen, paragraph [0046]).

Regarding claim 10, Wieczorek in view of Chen disclose the method for fabricating a CMOS transistor structure, comprising the steps of:

providing a semiconductor substrate having an N-type dopant region to support an PMOS transistor of the CMOS transistor structure and a P-type dopant region to support a NMOS transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure (Wieczorek et al., paragraph [0031] -- *Wieczorek et al discloses the invention is intended for forming CMOS transistor elements. CMOS transistor elements are understood in the art to be a pair of*

symmetrical complimentary transistors one p type and one n type. Wieczorek et al however only shows the general transistor structure, and does not disclose the obvious n/p type doping arrangement that is CMOS technology. It would be obvious to one of ordinary skill in the art that the CMOS structure mentioned by Wieczorek et al. would have a semiconductor substrate having a P-type dopant region to support an N-channel transistor of the CMOS transistor structure and an N-type dopant region to support a P-channel transistor of the CMOS transistor structure, each of the N-type dopant and P-type dopant regions having an overlying gate stack including a conductive gate structure and a dielectric gate structure, because this limitation is the fundamental structure of CMOS.)

forming lightly-doped extension regions in the semiconductor substrate adjacent each gate stack, the lightly-doped extension regions in the N-type dopant region (Wieczorek et al., Fig. 2d – [205]); comprising a P-type dopant having a dopant concentration in the range of about 1-2 e20 atoms/cm3 (Wieczorek et al., [0033-34]);

forming a layer of silicon oxide in contact with a total exposed surface of the lightly-doped extension regions (Wieczorek et al., [0033-34]);

forming an interfacial layer of nitrogen within the total exposed surface of botween the lightly-doped extension regions (Wieczorek et al., Fig. 2b);

the interfacial layer of nitrogen having an atomic nitrogen concentration in the range of 2-15 atomic percent (Wieczorek et al., [0034]);

forming at least one sidewall layer coupled to the layer of insulatinq material (Wieczorek et al., [0036] – not explicitly shown, however Wieczorek clearly discloses the spacers 209 can be comprised of a plurality of sidewall layers.);

forming source and drain regions in the semiconductor substrate adjacent to each of the gate stacks, the source and drain regions in the in the N-type dopant region comprising a P-type dopant having a concentration in the range of about 1-2 e20 atoms/cm3 (Wieczorek et al., Fig. 2C and [0033-34]);

Wieczorek et al. does not however disclose the additional step of forming a cap layer. This additional step was however known at the time of the invention to one of ordinary skill in the art. At the time of the invention it was known in that the induced strain/stress in the channel region of a CMOS device can be modified by performing an additional step of cap annealing. This know additional process step when forming a CMOS device is disclosed by Chen et al. Chen discloses the additional steps of:

forming a capping layer of contiguous silicon nitride having a thickness in the range of about 200-1000 angstroms over the semiconductor substrate; (Chen, Fig. 3 - [24] and paragraph [0048]).);

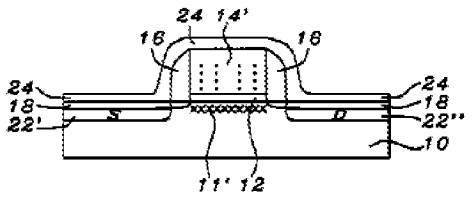

FIG. 3

annealing, after the formation of the capping layer and with the capping layer in place, the extension reqions and the source and drain regions at a temperature in the

range of 1000-1100 degrees centigrade for a period in the range of less than about 10 seconds (Chen, Fig. 4 - [27] paragraph [0051]); and

removing all of the capping layer after the annealing (Chen, Fig. 5 - [27] paragraph [0059]) – RTA will be less than 10 seconds);

It would have been within the scope of one of ordinary skill in the art at the time of the invention to combine the teachings of Wieczorek and Chen to enable the CMOS production step of Wieczorek to be performed according to the teachings of Chen because one of ordinary skill in the art at the time of the invention would have been motivated to look to alternative suitable methods of performing the disclosed CMOS production step of Wieczorek and art recognized suitability for an intended purpose has been recognized to be motivation to combine. MPEP § 2144.07.

Regarding claims 19 and 20, the prior art references Wieczorek and Chen are silent upon the step of breaking vacuum during the processing, therefore the Examiner take the position the prior art doe not teach "breaking vacuum" thus the process is understood to be performed without breaking vacuum.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Fernando L. Toledo/
Primary Examiner, Art Unit 2823

Jarrett J Stark
Examiner
Art Unit 2823

JJS
April 14, 2008